CLAIMS

1. A method for monitoring the mode of operation of one or more load circuits, especially of a domestic appliance, each containing a controlled semiconductor switch, especially a triac, and an electric consumer connected thereto, and which are supplied by at least one alternating voltage source, which supplies an alternating voltage comprising positive and negative voltage half-waves, characterised in that the currents flowing through all controlled semiconductor switches (T1, T2) and electric consumers (R1, R2) are guided through a common low-impedance precision resistor (Rm) and that the respective voltage drop occurring at this low-impedance precision resistor (Rm) is evaluated separately with respect to the amplitudes of the positive and negative voltage half-waves.

2. A circuit arrangement for carrying out the method according to claim 1 for monitoring the mode of operation of one or more load circuits, especially of a domestic appliance, each containing a controlled semiconductor switch, especially a triac, and an electric consumer connected thereto, and which are supplied by at least one alternating voltage source, which supplies an alternating voltage comprising positive and negative voltage half-waves, characterised in that all the electric consumers (R1, R2) together with their related controlled semiconductor switches (T1, T2) are connected via a low-impedance precision resistor (Rm) to the at least one alternating voltage source (Vac) and that an evaluation arrangement (Ed) which separately evaluates the positive and negative voltage half-waves of said alternating voltage is connected to said low-impedance precision resistor (Rm).

3. The circuit arrangement according to claim 2, characterised in that the evaluating arrangement (Ed) comprises a first evaluating device (Op1) which evaluates the positive voltage half-waves of the relevant alternating voltage and a second evaluating device (Op2) which evaluates the negative voltage half-waves of the relevant alternating voltage.

4. The circuit arrangement according to claim 3, characterised in that each of the two evaluating devices (Op1, Op2) is formed by an operational amplifier (Op1, Op2) which has its inverting input (-) and its non-inverting input (+) connected to the two ends of said low-impedance precision resistor (Rm).

5. The circuit arrangement according to claim 4, characterised in that a first operational amplifier (Op1) has its non-inverting input (+) and a second operational amplifier (Op2) has its inverting input (-) connected to one end of said precision resistor (Rm) and that said first operational amplifier (Op1) has its inverting input (-) and said second operational amplifier (Op2) has its non-inverting input (+) connected to the other end of said precision resistor (Rm).

6. The circuit arrangement according to claim 4 or claim 5, characterised in that connected to the outputs of the two operational amplifiers (Op1, Op2) is an evaluating circuit (Ec) which compares the output signals respectively delivered by the two operational amplifiers (Op1, Op2) with specified threshold voltages and which, depending on the magnitudes by which the output voltages respectively delivered by the relevant operational amplifiers (Op1, Op2) exceed or fall below said specified threshold voltages, delivers status signals which either indicate a correct current flow or a perturbed current flow through the respective electric consumers (R1, R2) and the controlled semiconductor switches (T1, T2) associated therewith.